

**WHAT IS CLAIMED IS:**

1. A method for insulating external surfaces of a multi-layer ceramic chip varistor device, comprising:  
coating a high insulating material on external surfaces of a multi-layer ceramic green compact;  
sintering the green compact into a ceramic body and forming an insulating layer on the ceramic body's surfaces;  
coating and sintering external electrodes onto the ceramic body in a sintering process; and  
extending internal electrodes inside the ceramic body by a heat treatment process to ensure a good electric contract between the internal and external electrodes.
2. The method according to Claim 1, wherein the heat treatment process causing the internal electrodes to extend and the sintering process of external electrodes can be combined and performed simultaneously to achieve a same result as the two processes are performed separately.
3. A method for insulating external surfaces of a multi-layer ceramic chip varistor device, comprising:  
coating a high insulating material on external surfaces of a ceramic body after the ceramic body is sintered but before the device's external electrodes are formed;  
forming an insulating layer on external surfaces of the ceramic body after the ceramic body is put through a heat treatment process;  
coating and sintering external electrodes onto the ceramic body in a sintering process; and

extending internal electrodes inside the ceramic body by a heat treatment process to ensure a good electric contract between the internal and external electrodes.

4. The method according to Claim 3, wherein the heat treatment process causing the internal electrodes to extend, the heat treatment process forming the insulating layer, and the sintering process of external electrodes can be combined and performed simultaneously to achieve a same result as the three processes are performed separately.

5. A method for insulating external surfaces of a multi-layer ceramic chip varistor device, comprising:

immersing the device's ceramic body in an acid or alkaline solution in a dip etching process after the ceramic body is formed but before the device's external electrodes are formed, during which the device's internal electrodes are exposed out of the ceramic body as the ceramic body is etched and shrunk;

coating a high insulating material on external surfaces of the ceramic body;

forming an insulating layer on external surfaces of the ceramic body after the ceramic body is put through a heat treatment process; and

coating and sintering external electrodes onto the ceramic body in a sintering process during which a good electric contact is established and ensured between the internal and external electrodes.

6. The method according to Claim 5, wherein the heat treatment process forming the insulating layer and the sintering process of external electrodes can be combined and performed simultaneously to achieve a same result as the two processes are performed separately.

7. A method for insulating external surfaces of a multi-layer ceramic chip varistor device, comprising:
- coating a high insulating material on external surfaces of the device after the device's ceramic body is formed, and after the device's external electrodes are formed in a sintering process, but before the external electrodes are plated with an electroplating process; and
- forming an insulating layer on external surfaces of the device after the device is put through a heat treatment process during which the insulating material on the external electrodes' surfaces is dissolved and blended with the external electrodes and the external electrodes still maintain a good conducting property.
8. The method according to Claim 7, wherein the heat treatment process forming the insulating layer and the sintering process of external electrodes can be combined and performed simultaneously to achieve a same result as the two processes are performed separately.
9. The method according to Claim 1, wherein the high insulating material is glass.
10. The method according to Claim 3, wherein the high insulating material is glass.
11. The method according to Claim 5, wherein the high insulating material is glass.
12. The method according to Claim 7, wherein the high insulating material is glass.
13. The method according to Claim 1, wherein the high insulating material is an organic compound.
14. The method according to Claim 3, wherein the high insulating material is an organic compound.
15. The method according to Claim 5, wherein the high insulating material is an organic compound.

16. The method according to Claim 7, wherein the high insulating material is an organic compound.
17. The method according to Claim 1, wherein the high insulating material is metallic oxide.
18. The method according to Claim 3, wherein the high insulating material is metallic oxide.
19. The method according to Claim 5, wherein the high insulating material is metallic oxide.
20. The method according to Claim 7, wherein the high insulating material is metallic oxide.
21. The method according to Claim 1, wherein the high insulating material is a metallic salt.
22. The method according to Claim 3, wherein the high insulating material is a metallic salt.
23. The method according to Claim 5, wherein the high insulating material is a metallic salt.
24. The method according to Claim 7, wherein the high insulating material is a metallic salt.
25. The method according to Claim 1, wherein the method is applied to insulate external surfaces of chip devices using a semiconducting or low insulating material as the devices' bodies.
26. The method according to Claim 3, wherein the method is applied to insulate external surfaces of chip devices using a semiconducting or low insulating material as the devices' bodies.

27. The method according to Claim 5, wherein the method is applied to insulate external surfaces of chip devices using a semiconducting or low insulating material as the devices' bodies.
28. The method according to Claim 7, wherein the method is applied to insulate external surfaces of chip devices using a semiconducting or low insulating material as the devices' bodies
29. The method according to Claim 1, wherein the heat treatment process causing the internal electrodes to extend has a characteristics that, after an insulating layer and external electrodes are formed on the device, the heat treatment process is conducted above 250°C causing Silver contained in the internal electrodes to be attracted out of the ceramic body by Silver contained in the external electrodes.
30. The method according to Claim 3, wherein the heat treatment process causing the internal electrodes to extend has a characteristics that, after an insulating layer and external electrodes are formed on the device, the heat treatment process is conducted above 250°C causing Silver contained in the internal electrodes to be attracted out of the ceramic body by Silver contained in the external electrodes.
31. The method according to Claim 5, wherein the dip etching process exposing the internal electrodes has a characteristics that, after the ceramic body is sintered but before an insulating layer is formed, the device is immersed in an acid or alkaline solution so that the ceramic body is etched and shrunk causing the internal electrodes to expose out of the ceramic body.

32. The method according to Claim 1, wherein the heat treatment process causing the internal electrodes to extend cal also be applied to chip devices using a semiconducting or low insulating material as the devices' bodies.
33. The method according to Claim 14, wherein the heat treatment process causing the internal electrodes to extend cal also be applied to chip devices using a semiconducting or low insulating material as the devices' bodies.
34. The method according to Claim 3, wherein the heat treatment process causing the internal electrodes to extend cal also be applied to chip devices using a semiconducting or low insulating material as the devices' bodies
35. The method according to Claim 15, wherein the heat treatment process causing the internal electrodes to extend cal also be applied to chip devices using a semiconducting or low insulating material as the devices' bodies.
36. The method according to Claim 4, wherein the dip etching process exposing the internal electrodes cal also be applied to chip devices using a semiconducting or low insulating material as the devices' bodies.
37. The method according to Claim 16, wherein the dip etching process exposing the internal electrodes cal also be applied to chip devices using a semiconducting or low insulating material as the devices' bodies.